

REMARKS

The present amendment is in response to the Office Action mailed September 29, 2003, in which Claims 1-5, 7-9, 17-19, 21 and 22 were rejected. Claims 6, 10-16, 20, and 23-28 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants have thoroughly reviewed the outstanding Office Action including the Examiner's remarks and the reference cited therein. The following remarks are believed to be fully responsive to the Office Action and, when coupled with the above amendments, are believed to render the claims at issue patentably distinguishable over the cited reference.

Claims 1-23 and 25-28 remain pending. Claims 1, 17, 20-21 and 25-28 are amended. Applicants respectfully submit that no new matter has been added and that the originally filed specification, drawings, and claims support the amendments.

Rejection of Claims 1-2, 4-5, 7, 9, 17, 19, 21 and 22 under 35 U.S.C. 102(b)

The Examiner has rejected Claims 1-2, 4-5, 7, 9, 17, 19, 21 and 22 under 35 U.S.C. §102(b), as being anticipated by Ker et al. (US#5,631,793). Applicants amend claims 1, 17 and 21 to overcome the rejection.

Ker et al. disclose a capacitor-couple electrostatic discharge (ESD) protection circuit for protecting an internal circuit and/or an output buffer of an IC from being damaged by an ESD current (Abstract). Ker's invention is an ESD protection circuit that consists of a PMOS transistor, a NMOS transistor and a potential leveling device (Claim 1 and figure 1). Therefore, there are two current routes provided in the Ker's invention for ESD events. Different ESD events can select different current route to bypass ESD event.

In contrast to the plurality of current routes, amended claim 1 only provides one current route for ESD events. In other words, only one current route is required to bypass different ESD events according to the present invention.

On the other hand, amended claim 17 discloses an ESD protection circuit that consists of two PMOS transistors and a RC controlled circuit (Claim 17 and figure 5). The amended claim 21 discloses an ESD protection circuit that consists of two NMOS transistors and two RC controlled circuits (Claim 21 and figure 6). Both ESD protection circuits are different from Ker's protection circuit that consists of a PMOS transistor, a NMOS transistor and a potential leveling device.

Nowhere in Ker is there taught or suggested that only one current route is required in different ESD events. And nowhere in Ker is taught or suggested that the protection circuit comprises two PMOS transistors or NMOS transistors. Thus, the subject matter as taught in amended claims 1, 17 and 21 would not be anticipated by Ker.

Rejection of Claims 3, 8, 18 and 22 under 35 U.S.C. 103(a)

Insofar as claims 3, 8, 18, and 22 respectively depend from independent claims 1, 17, and 21 and add further limitations thereto, they are patentable.

Accordingly, since the two inventions are different types of ESD protection circuit, it would not have been obvious based on the teachings of Ker to provide a protection circuit having the same structure as recited in amended claims 1, 17 and 21. Thus, the subject matter of amended claims 1, 17 and 21 are not obvious over Ker and therefore patentable over Ker. Likewise, by virtue of their dependence on patentable claims 1, 17 and 21, respectively, claims 2-16, 18-20 and 22-28 are also nonobvious and patentable over Ker.

Allowable Subject Matter

With respect to paragraph 5 at page 3 of the Office Action, the Examiner objected to Claims 20 and 23-28 as being dependent upon a rejected base claim, but Claims 20 and 23-28 would be allowable if rewritten in independent form including all of the limitations of the base claim and

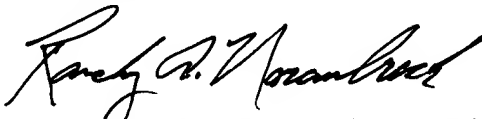
any intervening claims. Applicants accordingly amend Claims 17 and 21 by adding Claims 20 and 23-28 respectively to Claims 17 and 21. Applicants respectfully submits Claims 17 and 21 to be allowable.

Having overcome the rejections in the Office Acton, withdrawal of the rejections and expedited passage of the application to issue are requested. If there are any remaining issues to be resolved, the applicants request that the Examiner contact the undersigned attorney for a telephone interview.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 07-1337 and please credit any excess fees to such deposit account.

Respectfully submitted,

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